wherein the second input signal and the fourth input signal have an enable level during different periods from each other.

19. The display device of claim **18**, wherein the stage of the plurality of stages further comprises:

a second output transistor comprising a control end connected to the first node, a first end connected to the clock input end, and a second end connected to a second output end of the stage to output a carry signal; and

a third output transistor comprising a control end connected to the first node, a first end connected to the clock input end, and a second end connected to a third output end of the stage to output a compensation signal, and the second output transistor is back-biased by the compensation signal.

20. A gate driving circuit comprising:

a plurality of stages which outputs gate signals to corresponding gate lines,

wherein a stage of the plurality of stages comprises:

a first control transistor diode-connected between a first input end of the stage and a first node, wherein the first control transistor is biased by a first input signal of the first input end of the stage, and back-biased by a second input signal of a second input end of the stage;

a second control transistor comprising a control end connected to a third input end of the stage to receive a third input signal, a first end connected to the first node, and a second end connected to a first voltage, wherein the second control transistor is back-biased by a fourth input signal of a fourth input end of the stage;

a first output transistor comprising a control end connected to the first node, a first end connected to a clock input end of the stage, and a second end connected to a first output end of the stage;

a capacitor connected between a control end and a second end of the first output transistor;

a second output transistor comprising a control end connected to the first node, a first end connected to the clock input end, and a second end connected to a second output end of the stage to output a carry signal;

a first inverter transistor connected to a first voltage having a lower voltage level than a low level of the gate signals, where the first inverter transistor transmits the first voltage to the second node during a period during which the carry signal is output; and

a second inverter transistor connected to a second voltage having a same voltage level as the low level of the gate signals, wherein the second inverter transistor is turned off during a period other than the period during which the carry signal is output,

wherein the second input signal and the fourth input signal have an enable level during different periods from each other.

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